Amendments to the Claims:

Please amend claims 3 and 9 as follows:

1. (Previously Presented) A Vestigial Sideband (VSB) transmission system comprising:

a supplemental data processor processing supplemental data including Reed-Solomon encoding, inserting a plurality of null bits , and inserting an MPEG header;

a first multiplexer multiplexing MPEG data and said data processed in said supplemental data processor;

a data encoding part processing said multiplexed data including data randomizing, adding a first Reed-Solomon parity, data interleaving, and byte-symbol converting in order to generate an input data symbol;

a supplemental data symbol processor encoding an information bit of said input data symbol with a 1/2 coding rate;

a data decoding part processing said data processed in said supplemental data symbol processor including symbol-byte converting, data de-interleaving , eliminating said first Reed-Solomon parity added in said data encoding part; and

a VSB transmitter processing said data processed in said data decoding part including trellis encoding, adding a second Reed-Solomon parity, data interleaving, VSB modulating, and transmitting to a receiving side.

2. (Original) The VSB transmission system of claim 1 further comprising a control signal generator generating a first control signal indicating whether said input data symbol is a supplemental data symbol and generating a second control signal based on said first control signal, said control signal generator providing said control signals to said supplemental data symbol processor.

3. (Currently amended) The VSB transmission system of claim 2, wherein said supplemental data symbol processor comprises:

a 1/2 rate convolutional encoder outputting said information bit as a first output bit and encoding said information bit with said 1/2 coding rate to generate a third parity bit; and

a second multiplexer multiplexing said third parity bit with ~~the~~ a null bit based on said second control signal in order to generate a second output bit.

4. (Original) The VSB transmission system of claim 2, wherein said second control signal is a puncturing control signal having a puncturing pattern being repeated.

5. (Original) The VSB transmission system of claim 3, wherein said 1/2 rate convolutional encoder comprises:

a first set of multipliers $G_1, G_2, G_3, \ldots G_{M-1}$, wherein G_i multiplies said information bit with its given constant g_i;

a second set of multipliers $H_1, H_2, H_3, \ldots H_{M-1}$, wherein H_i multiplies a previous third parity bit value with its given constant h_i;

a set of registers $r_1, r_2, r_3, \ldots r_{M-1}, r_M$, wherein r_M stores said previous third parity bit value and r_i stores a value obtained by adding outputs from G_i, H_i, and r_{i+1}; and

a set of adders, wherein an i th adder adds said outputs from G_i, H_i, and r_{i+1}, where $g_i, h_i \in \{0,1\}$, $i = M-1, \ldots 3,2,1$, and the value being stored in r_1 is output as said third parity bit.

6. (Original) The VSB transmission system of claim 3, wherein said 1/2 rate convolutional encoder comprises:

a first register storing a previous third parity bit value;

an adder adding said value stored in said first register and said information bit of said input data symbol; and

a second register storing said added value, where said value stored in said second register is output as said third parity bit.

7. (Original) The VSB transmission system of claim 3, wherein said 1/2 rate convolutional encoder comprises:

a first register storing a previous third parity bit value;

a first adder adding said value stored in said first register and said information bit of said input data symbol;

a second register storing said value added by said first adder;

a second adder adding said value stored in said second register and said previous third parity bit value; and

a third register storing said value added by said second adder,

where said value stored in said third register is output as said third parity bit.

8. (Original) The VSB transmission system of claim 3, wherein said 1/2 rate convolutional encoder comprises:

a first register storing a previous third parity bit value;

a first adder adding said value stored in said first register and said previous third parity bit value;

a second register storing said value added in said first adder;

a second adder adding said value stored in said second register and said information bit of said input data symbol;

a third register storing said value added in said second adder; and

a fourth register storing said value stored in said third register,

where said value stored in said fourth register is output as said third parity bit.

9. (Currently amended) The VSB transmission system of claim 2, wherein said supplemental data symbol processor comprises:

a first selecting element selecting a previous second register value if said first control signal indicates that said input data symbol is said supplemental data symbol and otherwise selecting a previous first register value;

a first register storing said value selected by said first selecting element;

an adder adding said value stored in said first register and said information bit of said input data symbol;

a second selecting element selecting said value added by said adder if said first control signal indicates that said input data symbol is said supplemental data symbol and otherwise selecting said previous second register value;

a second register storing said value selected by said second selecting element;

a third selecting element selecting said value stored in said second register if said second control signal indicates that said input data symbol is said supplemental data symbol and otherwise selecting ~~said~~ a null bit ; and

a fourth selecting element selecting said value selected by said third selecting element if said first control signal indicates that said input data symbol is said supplemental data symbol and otherwise selecting ~~said~~ a null bit ,

said information bit being output as a first output bit, said value selected by said fourth selecting element being output as a second output bit, and said previous first and second register values being values previously stored in said first and second registers, respectively.

10-18. (Canceled)